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10/727,181	12/02/2003	Richard Thomas Plunkett	PEA01US	6713

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EXAMINER	
KAU, STEVEN Y	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/727,181	PLUNKETT ET AL.	
	Examiner	Art Unit	
	STEVEN KAU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Applicant's amendment was received on 9/10/2009, and has been entered and made of record.

Status of the Claims

2. Claims 1-6 are pending for further examination in this Action.

Response to Remark/Arguments

3. Applicant's arguments with respect to the rejection of claims 1-6 under 35 U.S.C. 103(a) have been fully considered but are not persuasive. Thus, same ground of rejection is remained and still stands. Reply to applicant's remarks/arguments is discussed below.

Applicant's arguments, "It is respectfully submitted that the Examiner has misunderstood the teachings of Hashimoto. In asserting that the combination of references teaches the feature of 'steps (a) to (c) are performed simultaneously with step (d)', the Examiner refers to Hashimoto at col. 6, lines 31 - 40. Having reviewed the entirety of Hashimoto, however, it is clear to Applicant that the 'simultaneous' feature of Hashimoto refers not to a simultaneity between reading and writing data from/into the line buffers. Rather, the simultaneity achieved in Hashimoto is in being able to simultaneously perform a read or a write while the DRAM memory is being refreshed."

"This is clear firstly when the description at col. 6, lines 31 - 40, is read in its entirety. Col. 6, lines 31 - 40 states that 'simultaneous generation of write, read, and refresh request signals' can be accommodated without interrupting data read out from said read line buffer memory to perform a refresh of said dynamic memory cells of said dynamic memory array...' . This is further clear from the description at col. 3, lines 14 - 22, where it is described that 'If line buffers are built in... and if necessary data is.., read...serially through a line buffer .... there will be no practical difficulty in reading data...if a read request signal is generated during the refresh mode... '".

In re, the Examiner respectfully disagrees with applicant's argument present above. With respect to Claim 1, the independent claim of the invention, is directed to a method for sequentially outputting full lines of dither values of a dither matrix stored in a memory (emphasis added by the examiner). Steps of the method recite, ***"(a) reading a plurality of dither values of the dither matrix from the memory into a buffer memory, the reading commencing at a start position in the memory until a full line of dither values of the dither matrix has been read; (b) updating the start position to an updated start position in the memory of a subsequent line of dither values; (c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory; (e) repeating steps (a) - (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory, wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d)***." Thus, the claimed invention as a whole, is to read and write matrix values of a dither matrix, or a matrix, or an array stored in a memory, i.e. a line buffer memory. As discussed in the previous

Action, the primary prior art, Shu (US 5,594,839) discloses a method for sequentially outputting full lines of dither values of a dither matrix stored in a memory (**e.g. dither process for image reproduction and full lines of dither value are outputted from a memory, e.g. memory 738 of Fig. 7 in a sequential order, i.e. lines of dither value is controlled by pixel address, col 10, lines 15-34**), comprising the steps of: (a) reading a plurality of dither values of the dither matrix from the memory into a buffer memory (**referring to Fig. 7, dither values are outputting to buffer memory 710), the reading commencing at a start position in the memory until a full line of dither values of the dither matrix has been read (i.e. identifying a line in the dither array with address for halftone process; thus each time a line is retrieved from ROM, a start position of the line in the ROM is adjusted, or commenced, col 10, lines 23-44**);

(b) updating the start position to an updated start position in the memory of a subsequent line of dither values (**e.g. since more than one dither lines are stored in the dither array, thus the next to the current line being processed must be updated to be a new line in order to continue for halftone processing, col 10, lines 35-48**);

(e) repeating steps (a) - (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory (**e.g. halftone processing is perform pixel by pixel; in addition, dither array is smaller than the image array and during dither process, dither array is repeated side by side over the image array to produce**

repetitive pattern, thus iteration of steps (a) to (c) must be performed, col 8, lines 10-23).

Shu does not disclose (c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory; and wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d).

Prior art Schmidt (US 5,193,012) teaches (c) outputting the full line of dither values into the buffer memory (**referring to Fig. 4, Step 59, "load half-tone Facsimile Pixel into Facsimile Multi- line Buffer", and col 4, lines 17-19, & again in col 11, lines 18-22**); (d) outputting a full line of dither values from the buffer memory (**i.e. half-tone facsimile lines are sequentially read out of the multi-line buffer, col 4, 20-23**), said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory (**referring to Fig. 4, Steps 61, 64 and 65, "reset second facsimile line, first dot-position" and "transmit a facsimile line in facsimile multi- buffer", and col 11, lines 31-49**); and

Prior art Hashimoto (US 4,999,814) teaches wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d) (**i.e. simultaneous generation of write, read and refresh can be achieved for read/write line buffer memory, col 6, lines 31-40**).

Having a method of Shu' 839 reference and then given the well-established teaching of Schmidt' 012 reference, it would have been obvious to one having ordinary

skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include (c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory as taught by Schmidt' 012 reference since doing so would have been increase the versatility of the method, i.e. better synchronization in loading and outputting halftone or dither values; and then to modify the combination of Shu and Schmidt to include wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d) as taught by Hashimoto' 814, since doing so would have been to improve the method efficiency and save process time, and further the services provided could easily be established for one another with predictable results.

As we can see, the invention is obvious to Shu '839 in view of prior arts of Schmidt' 012, and Hashimoto' 814.

However, applicant argues that prior art Hashimoto' 814 does not teach "steps (a) to (c) are performed simultaneously with step (d)", and the examiner found this argument is not persuasive. First, prior art Hashimoto '814 discloses a circuit configuration of a semiconductor memory device of Fig. 1, which includes including a dynamic memory array having a plurality of dynamic memory cells arranged in a matrix of rows and columns, write line and read line buffer memories disposed at the input and output of the dynamic memory array. Furthermore, prior art Hashimoto' 814 discloses "**In FIG. 1, for sake of descriptional convenience, it is assumed that 200 parallel**

sense amplifiers are provided in the direction of row of dynamic memory elements with the write line buffer and read line buffer connected to these sense amplifiers for parallel input and output, respectively" (col 1, lines 61-66) and "this memory device is equipped with a pair of line buffers for serial-parallel and parallel-serial conversion of write and read data", "Data is written by the following sequential of steps (1) to (6)", (see col 2, lines 10-51), i.e. "At the start of the 101th data write cycle after the 100th data has been written", "After the data No. 200 has been written, the write pointer returns back (or updating the start position) to the address No. 1 to write data from this address and at the same time a signal WRQ is generated to set the WACT and .phi.w2 true by the same procedure", etc., (see col 2, lines 10-51); and to read data, "data Nos. 1 to 100 are stored beforehand to the read line buffer and a read request signal RRQ is generated at the timing when the data No. 1 is read out", etc., (see col 2, lines 53-62). Thus, given a circuit structure of a semiconductor memory device and its function of write/read values of a matrix or an array in parallel input and output, and the teaching of "**said write line buffer memory and said read line buffer memory being provided with a bit storage capacity of sufficient size such that the simultaneous generation of write, read, and refresh request signals can be accommodated without interrupting data read out from said read line buffer memory to perform a refresh of said dynamic memory cells of said dynamic memory array in response to the refresh request signal, whereby a substantially refresh-free serial data access memory is provided" (col 6, lines 31-40);** the limitation of "steps (a) to (c) are performed simultaneously with step (d)". Therefore, the

invention as a whole is obvious to Shu '839 in view of prior arts of Schmidt' 012, and Hashimoto' 814. And the examiner believes the rejection of claims 1-6 in the previous Action is proper and the same ground of rejection is therefore maintained and still stands.

In accordance with 37 U.S.C. 1.173(c), which requires that "Whenever there is an amendment to the claim pursuant to paragraph (b) of this section, there must also be supplied, on pages separate from the pages containing the changes, the status (i.e. pending or canceled), as of the date of the amendment, of all patent claims and of all added claims, and an explanation of the support in the disclosure of the patent for the changes made to the claims", the examiner requests the applicants to provide supports of "(d) repeating steps (a)- (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory, wherein after a first iteration of steps (a) - (c), steps (a) and (c) are performed simultaneously" in the original specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) in view of Schmidt (US 5,193,012) and Hashimoto (US 4,999,814).

Regarding claim 1.

Shu discloses a method for sequentially outputting full lines of dither values of a dither matrix stored in a memory (**e.g. dither process for image reproduction and full lines of dither value are outputted from a memory, e.g. memory 738 of Fig. 7 in a sequential order, i.e. lines of dither value is controlled by pixel address, col 10, lines 15-34**), comprising the steps of: (a) reading a plurality of dither values of the dither matrix from the memory into a buffer memory (**referring to Fig. 7, dither values are outputting to buffer memory 710**), the reading commencing at a start position in the memory until a full line of dither values of the dither matrix has been read (**i.e. identifying a line in the dither array with address for halftone process; thus each time a line is retrieved from ROM, a start position of the line in the ROM is adjusted, or commenced, col 10, lines 23-44**);

(b) updating the start position to an updated start position in the memory of a subsequent line of dither values (**e.g. since more than one dither lines are stored in**

the dither array, thus the next to the current line being processed must be updated to be a new line in order to continue for halftone processing, col 10, lines 35-48);

(e) repeating steps (a) - (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory (**e.g. halftone processing is perform pixel by pixel; in addition, dither array is smaller than the image array and during dither process, dither array is repeated side by side over the image array to produce repetitive pattern, thus iteration of steps (a) to (c) must be performed**, **col 8, lines 10-23**).

Shu does not disclose (c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory; and wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d).

Schmidt teaches (c) outputting the full line of dither values into the buffer memory (**referring to Fig. 4, Step 59, "load half-tone Facsimile Pixel into Facsimile Multi-line Buffer", and col 4, lines 17-19, & again in col 11, lines 18-22**); (d) outputting a full line of dither values, or matrix values from the buffer memory (**i.e. half-tone facsimile lines are sequentially read out of the multi-line buffer, col 4, 20-23**), said outputting of dither values or matrix values from the buffer memory commencing after a full line of dither values has been output into the buffer memory (**referring to Fig. 4,**

Steps 61, 64 and 65, "reset second facsimile line, first dot-position" and "transmit a facsimile line in facsimile multi-buffer", and col 11, lines 31-49); and

Hashimoto teaches wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d) (**prior art Hashimoto '814 discloses a circuit configuration of a semiconductor memory device of Fig. 1, which includes including a dynamic memory array having a plurality of dynamic memory cells arranged in a matrix of rows and columns, write line and read line buffer memories disposed at the input and output of the dynamic memory array. Furthermore, prior art Hashimoto' 814 discloses "In FIG. 1, for sake of descriptional convenience, it is assumed that 200 parallel sense amplifiers are provided in the direction of row of dynamic memory elements with the write line buffer and read line buffer connected to these sense amplifiers for parallel input and output, respectively**", (col 1, lines 61-66) and "this memory device is equipped with a pair of line buffers for serial-parallel and parallel-serial conversion of write and read data", "Data is written by the following sequential of steps (1) to (6)", (see col 2, lines 10-51), i.e. "At the start of the 101th data write cycle after the 100th data has been written", "After the data No. 200 has been written, the write pointer returns back (or updating the start position) to the address No. 1 to write data from this address and at the same time a signal WRQ is generated to set the WACT and .phi.w2 true by the same procedure", etc., (see col 2, lines 10-51); and to read data, "data Nos. 1 to 100 are stored beforehand to the read line buffer and a read request signal RRQ is generated at the timing when the data No. 1 is read out", etc., (see col 2, lines 53-62).

Thus, given a circuit structure of a semiconductor memory device and its function of write/read values of a matrix or an array in parallel input and output, and the teaching of **"said write line buffer memory and said read line buffer memory being provided with a bit storage capacity of sufficient size such that the simultaneous generation of write, read, and refresh request signals can be accommodated without interrupting data read out from said read line buffer memory to perform a refresh of said dynamic memory cells of said dynamic memory array in response to the refresh request signal, whereby a substantially refresh-free serial data access memory is provided" (col 6, lines 31-40), the limitation is taught and suggested by Hashimoto**).

Having a method of Shu' 839 reference and then given the well-established teaching of Schmidt' 012 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to apply the known technique of "(c) outputting the full line of dither values into the buffer memory; (d) outputting a full line of dither values from the buffer memory, said outputting of dither values from the buffer memory commencing after a full line of dither values has been output into the buffer memory" as taught by Schmidt' 012 reference since doing so would have been increase the versatility of the method, i.e. better synchronization in loading and outputting halftone or dither values; and then to modify the combination of Shu and Schmidt to include wherein after a first iteration of steps (a) - (c), steps (a) to (c) are performed simultaneously with step (d) as taught by Hashimoto' 814, since doing so would have been to improve the method efficiency and

save process time, and further the services provided could easily be established for one another with predictable results.

Regarding claim 6, in accordance with claim 1.

Shu does not disclose wherein step (d) is performed at a rate faster than step (a).

Hashimoto teaches wherein step (d) is performed at a rate faster than step (a) (**i.e. read/write control of DRAM has been a task, i.e. Fig. 21 of the specification of the current application, and Hashimoto discloses that assuming 30 nsec for maximum bit rate for serial data writing or reading and 300 nsec for cycling, thus, outputting one full line from a buffer is for sure faster than step (a) of the current invention, col 3, lines 1-36**).

Having a method of Shu' 839 reference and then given the well-established teaching of Hashimoto' 814 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include wherein step (d) is performed at a rate faster than step (a), since doing so would have improve the control of data processing in between memories and buffers.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) in view of Schmidt (US 5,193,012 and Hashimoto (US 4,999,814) as applied to claim 1 above, and further in view of Young et al (US 6,154,195).

Regarding claim 4, in accordance with claim 1.

Shu' 839 does not disclose wherein, in repeated step (b), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position.

Young' 195 teaches wherein, in repeated step (b), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position (**Young' 195 teaches outputting dither values to a buffer memory line by line in step (b), thus, the end of each line must be determined and a new line must be updated in order to have the halftone process performed properly, Fig. 3, col 7, lines 47-50**).

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Young' 195 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include in repeated step (b), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position as taught by Young' 195 reference since doing so would ensure the dither/half-tone performed properly and further outputting dither values to a buffer memory and updating line input provided by Young' 195 could easily be established for one another with predictable results.

8. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) in view of Schmidt (US 5,193,012 and Hashimoto (US

4,999,814) as applied to claim 1 above, and further in view of Yamashita et al (US 5,701,505).

Regarding claim 2, in accordance with claim 1.

Shu does not explicitly disclose wherein a plurality of dither matrices are stored in the memory, and wherein step (a) includes reading a plurality of dither values from at least two of the dither matrices simultaneously.

Yamashita discloses wherein a plurality of dither matrices are stored in the memory (**e.g. dither matrices are contained in the halftone circuits, which implies that dither matrices are stored in the memory of the circuitry, col 20, line 43 through col 21, line 11**), and wherein step (a), includes reading a plurality of dither values from at least two of the dither matrices simultaneously (**e.g. Yamashita discloses a parallel processing apparatus which processing data in block cycles, i.e. Fig. 27 teaches a process of outputting 4 lines; in order to support the parallel processing, the halftone-processing circuits 751-754 must reading at least two of the dither matrices simultaneously as shown in Figs 32-25 & col 20, line 63 through col 21, line 11**).

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Yamashita' 505 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Shu' 839, Schmidt' 012 and Hashimoto' 814 to include a plurality of dither matrices are stored in the memory, and wherein step (a) includes reading a plurality of dither values from at least two of the

dither matrices simultaneously as taught by Yamashita' 505 reference since doing so would have been to improve the processing efficiency of reading and outputting dither values in and out of memory to reducing processing time, and further, the concept of parallelism can be implemented with a predictable result.

Regarding claim 5, in accordance with claim 2.

Claim 5 recites identical features as claim 4. Thus, arguments similar to that presented above for claim 4 are also equally applicable to claim 5.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) in view of Schmidt (US 5,193,012 and Hashimoto (US 4,999,814), and further in view of Yamashita et al (Yamashita) (US 5,701,505) as applied to claim 2 above, and further in view of Matsuba et al (Matsuba) (US 5,815,286).

Regarding claim 3, in accordance with claim 2.

Shu' 839 does not disclose wherein the dither matrices are of different sizes.

Matsuba' 286 discloses wherein the dither matrices are of different sizes (**e.g. four color components can be processed with respect to four threshold matrices value at the same time**, **Figs. 1a-c & col 7, lines 9-18 and col 20, lines 21-32**).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the combination of Shu' 839, Schmidt' 012, Hashimoto' 814 and Yamashita' 505 to include that dither matrices are of different sizes taught by Matsuba' 286 and therefore, four color components can be processed with

respect to four threshold matrices value at the same time (Figs 21A-D, col 20, lines 21-32).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Kau whose telephone number is 571-270-1120 and fax number is 571-270-2120. The examiner can normally be reached on Monday to Friday, from 8:30 am -5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Steven Kau/
Examiner, Art Unit 2625
November 21, 2009

/David K Moore/

Supervisory Patent Examiner, Art Unit 2625